REMARKS

Claims 1, 3 and 6-26 are pending in this application. Of these, claims 3 and 19 were objected to and are cancelled herein. Claims 1, 16-18, 20 and 22-26 have been amended and claim 27 is added herein. Applicants respectfully request reconsideration of the claims in view of the following remarks.

Applicants gratefully acknowledge allowance of claims 11-13, 15, 17 and 21.

Applicants have revised Figure 8 to include reference number 66 as shown on the attached sheet labeled "Annotated Marked-Up Drawing". A clean "Replacement Sheet" will follow.

Claims 22-26 were rejected under 35 U.S.C. §112, first paragraph, as not having sufficient support in the specification to show the inventor had possession of the claimed invention. More specifically, the Examiner alleges that the limitation of "an electrical conductor" (recited in the base independent claims 1, 6, 18 and 20) being formed on a printed circuit board as required by claims 22-26 is not supported by the original disclosure. Further, the Examiner states that the "electrical conductor structure is disposed on "a semiconductor wafer," but not disposed on "a printed circuit board" as recited in the new claims 22-26.

Applicants strongly disagree and refer the Examiner to the paragraph bridging page 6, lines 22-34 and page 7, lines 1-15 of the specification along with figures 6 and 7. Specifically, dielectric member 49 and patterned electrical conductor(s) 52 on one (the inner) surface of the dielectric member 49 is clearly described at lines 23-25 of page 6 of the specification as a "thin printed circuit board." Figure 6 clearly illustrates the printed circuit board combination of

dielectric member 49 and conductor 52 prior to being joined to the fabricated semiconductor wafer 30 as indicated by the large space (no reference number) between the conductor 52 and the contacts 53 of the wafer 30 and as discussed at lines 4-8 on page 7 of the specification.

Figure 7 illustrates a package structure 60 after the combination of dielectric member 49 and conductor 52 has been joined with the semiconductor wafer 30 and sliced or separated. More specifically, as clearly shown in figure 7, and/or discussed at lines 9-15 of page 7, the conductor 52 on the dielectric member 49 is electrically connected to the contacts 53 on semiconductor wafer 30 through connections 54 (e.g., solder bump connections) which maintain the dielectric member 49 at a small spaced distance above the semiconductor wafer 30 as the conductor 52 "spans" the separating regions 33 (page 7, line 6 and 14).

Therefore, it is respectfully submitted that the Examiner's position that the electrical conductor structure "is disposed on a semiconductor wafer but not disposed on a printed circuit board" as recited in the claims is simply incorrect and the 112 rejection should be withdrawn. It is also noted that the rejected independent claims 1, 6, 16, 18 and 20 have been amended to clarify this structures.

It should also be noted that there is a second printed circuit board 66 in addition to the printed circuit board combination of dielectric member 49 and conductor 52. As discussed at lines 16-22 of page 7 and illustrated in Figure 8, second printed circuit board 66 having interconnects 68 is used to form a "memory module 62" comprised of a plurality of the package structure 60 discussed above.

Claims 1, 6 and 7 were rejected under 35 U.S.C. §102(b) as being fully anticipated by both the Saitou, *et al.* and Murari, *et al.* references.

However, independent claims 1 and 6 now clearly include limitations that are in no way even discussed much less taught by either Saitou, *et al.* or Murari, *et al.* More specifically, neither of the references teaches a planar dielectric member and conductor, such as a printed circuit board, spaced from the semiconductor wafer that spans the separating regions in the wafer and connects to circuit chips and/or electrical components.

Therefore, it is respectfully submitted that claims 1, 6 and 7 are not anticipated under 35 U.S.C. §102 and are allowable.

Claims 16, 18, 20 and 22-26 were rejected under 35 U.S.C. §103(a) as being unpatentable over Saitou, *et al.* or Murari, *et al.* in view of Barth, *et al.* However, independent claims 16, 18 and 20 have also been amended to include the same limitation as discussed above with respect to independent claims 1 and 6 rejected under 35 U.S.C. §102. Further, the Barth, *et al.* reference includes no teaching of the dielectric member and conductor being spaced from the semiconductor wafer that would overcome the shortcomings of the Saitou, *et al.* and Murari, *et al.* references. Therefore, it is submitted there these independent claims are also allowable. Dependent claims 22-26 all depend from claims deemed allowable and are therefore allowable for depending on an allowable claim as well as for their own limitations.

Claims 3 and 19 were objected to as being dependent upon a rejected claim, but were indicated as allowable if rewritten in independent form. Claims 3 and 19 were cancelled and their limitations were included in new independent claims 27 and 28.

Therefore, it is respectfully submitted that all of the claims now in the case are patentable and the Examiner is urged to pass the case is issue.

Respectfully submitted,

19 Jan 2004
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